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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,942	03/22/2004	Isaac Kantorovich	200310359-1	1037

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EXAMINER
KRAMSKAYA, MARINA

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/805,942	KANTOROVICH ET AL.	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10-13,18-20 and 25-27* is/are rejected.

7)☒ Claim(s) *2-9,14-17 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 11-12, 13, 18-19, 20, & 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Osburn et al., US 6,472,899.

As per Claim 1, Osburn discloses a method, comprising:

- determining a worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages) of a power supply loop coupled to a power input (Power Supply, indicated as PS in FIG. 1) of a die (Integrated circuit, IC **102**);
- determining a reference voltage (block 202 in FIG. 2) at the power input of the die associated with an average current generated at a power supply included in the power supply loop;
- measuring a maximum change in a current (column 5, lines 22-28, see FIG. 3) at the power input of the die; and

- calculating an estimate of a worst-case voltage (column 4, lines 1-5) at the power input of the die based upon the worst-case impedance, the reference voltage, and the maximum change in the current.

As per Claims 11 and 12, Osburn further discloses calculating an estimate of a maximum worst-case voltage (block 206) and a minimum worst-case voltage (block 208).

As per Claim 13, Osburn discloses a computer program embodied in a computer readable medium (column 12, line 64 - column 13, line 7), comprising:

- code that determines a worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages) of a power supply loop coupled to a power input Power Supply, indicated as PS in FIG. 1) of a die (Integrated circuit, IC **102**); and
- code that calculates an estimate of the worst-case voltage (column 4, lines 1-5) at the power input of the die based upon a number of factors, including:
    - the worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages);
    - an estimated maximum change in a current at the power input of the die (column 5, lines 22-28, see FIG. 3); and

- a reference voltage (block 202 in FIG. 2) at the power input of the die, the reference voltage being associated with an average current generated at a power supply included in the power supply loop.

As per Claims 18 and 19, Osburn further discloses a code for calculating an estimate of a maximum worst-case voltage (block 206) and a minimum worst-case voltage (block 208).

As per Claim 20, Osburn discloses a system (column 12, line 64 - column 13, line 7) for determination of a worst-case voltage, comprising:

- a processor circuit having a processor and a memory (column 12, line 63);
- a worst-case voltage (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages)calculator stored in the memory and executable by the processor (column 12, line 63), the worst-case voltage calculator comprising:
  - logic that determines a worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages) of a power supply loop coupled to a power input (Power Supply, indicated as PS in FIG. 1) of a die(Integrated circuit, IC **102**); and
  - logic that calculates an estimate of the worst-case voltage (column 4, lines 1-5) at the power input of the die based upon a number of factors, including:

- the worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages);
- an estimated maximum change in a current (column 5, lines 22-28, see FIG. 3) at the power input of the die; and
- a reference voltage (block 202 in FIG. 2) at the power input of the die, the reference voltage being associated with an average current generated at a power supply included in the power supply loop.

As per Claims 25 and 26, Osburn further discloses logic for calculating an estimate of a maximum worst-case voltage (block 206) and a minimum worst-case voltage (block 208).

As per Claim 27, Osburn discloses a system for determination of a worst-case voltage, comprising:

- means for determining a worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages) of a power supply loop coupled to a power input (Power Supply, indicated as PS in FIG. 1) of a die (Integrated circuit, IC **102**); and
- means for calculating an estimate of the worst-case voltage (column 4, lines 1-5) at the power input of the die based upon a number of factors, including:
    - the worst-case impedance (minimum and maximum load line slopes of FIG. 3, are associated with the worst case voltages);

- o an estimated maximum change in a current (column 5, lines 22-28, see FIG. 3) at the power input of the die; and
- o a reference voltage (block 202 in FIG. 2) at the power input of the die, the reference voltage being associated with an average current generated at a power supply included in the power supply loop.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Osburn, in view of Sakaguchi, US 5,949,798.

Osburn discloses a method of testing as applied to Claim 1 above.

Osburn does not disclose the measurement of the maximum change in the current at the power input of the die further comprising:

- executing an aggressive process on the die; and
- measuring and storing the current at the power input of the die as a function of time.

Sakaguchi discloses the measurement of the maximum change in the current at the power input of the die further comprising:

- executing an aggressive process on the die (test pattern: block **301** in FIG. 2); and

  measuring and storing **6** the current at the power input of the die as a function of time (block **302**, FIG. 2).

Therefore, it would have been obvious to a person of ordinary skill in the art to execute an aggressive process in the die and measure and store the current, as taught by Sakaguchi, in the testing method of Osburn, in order to determine troubles in the integrated circuit or die.

Allowable Subject Matter

5. Claims 2-9, 14-17, & 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to teach a method and a system for determining the worst case impedance on a die characterized in:

measuring a voltage V(t) at the power input of the die while executing an alternating hot and cold process on the die, wherein the alternating hot and cold process generates a current at the power input of the die that approximates a periodic waveform;

identifying a pre-transition voltage before a half-period of the voltage V(t), and a number of maximum voltages and a number of minimum voltages of a response of the voltage V(t) within the half-period of the voltage V(t);

determining a period of the alternating hot and cold process to be at least as great as X/f1, where f1 is defined as a frequency of a right-most peak corresponding to a resonance in the power supply loop as depicted in a graph of the impedance of the power supply loop as a function of frequency, and X is specified so as to include the maximum voltages and the minimum voltages within the half-period of the voltage V(t), wherein the maximum and minimum voltages comprise all significant maximum voltages and all significant minimum voltages of the response of the voltage V(t); and

calculating the worst-case impedance using the equation

$$R_w = \frac{\sum_{i=0}^{M} |V_{2i} - V_{2i+1}|}{\Delta I_{dd}},$$

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Beasley et al., US 5,483,170, and Teene, US 5,726,997, disclose a method of testing integrated circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571)272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marina Kramskaya
Examiner
Art Unit 2858
M. Kramskaya

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V. Nguyen
5/02/2005

VINCENT Q. NGUYEN
PRIMARY EXAMINER